AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A method of detecting a reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor is not parametrically affected by a reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said

second MOS transistor is parametrically affected by said reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said reticle option layer in said integrated circuit device.

2. (Original) The method according to Claim 1 wherein said reticle option layer comprises a threshold voltage implantation.

3. (Original) The method according to Claim 1 wherein said reticle option layer comprises one of the group of: polysilicon, metal, and threshold implantation.

4. (Original) The method according to Claim 1 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

5. (Original) The method according to Claim 1 wherein said reticle option layer comprises a combination of reticle layers.

6. (Original) The method according to Claim 5 wherein said combination of reticle layers comprises the group of: polysilicon, metal, and threshold implantation.

7. (Original) The method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by directly probing the die of said integrated circuit device.

8. (Original) The method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said integrated circuit device.

9. (Original) The method according to Claim 1 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

10. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor has both said first threshold voltage implantation and said threshold voltage implantation reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

11. (Original) The method according to Claim 10 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

12. (Original) The method according to Claim 10 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by directly probing the die of said integrated circuit device.

13. (Original) The method according to Claim 10 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said integrated circuit device.

14. (Original) The method according to Claim 10 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

15. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first NMOS transistor to an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of said first NMOS transistor is connected to ground, and wherein said first NMOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when an internal test voltage is connected to said drain and said gate of said first NMOS transistor through a first internal standard resistance;

selecting a second NMOS transistor in said integrated circuit device in a second test mode to couple the voltage at the drain and the gate of said second NMOS transistor to said output pin of said integrated circuit device wherein said gate and said drain of said second NMOS transistor are connected together, wherein the source of said NMOS transistor is connected to ground, and wherein

said second NMOS transistor has both said first threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said internal test voltage is connected to said drain and said gate of said second NMOS transistor through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

16. (Original) The method according to Claim 15 wherein said selecting of said first NMOS transistor is by a multiplex circuit and wherein said selecting of said second NMOS is by a multiplex circuit.

17. (Original) The method according to Claim 15 further comprising amplifying said voltage at said drain and said gate of said first NMOS transistor and said second NMOS transistor to thereby generate an amplified drain and gate voltage at said output pin.

18. (Original) The method according to Claim 15 wherein said first NMOS transistor and said second NMOS transistor are the same size, the same layout orientation, and in close proximity.

19. (Original) The method according to Claim 15 wherein said first internal resistance and said second internal resistance comprise the same resistance value.

20. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first PMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first PMOS transistor to an output pin of said integrated circuit device wherein said gate and said drain of said first PMOS transistor are connected together, wherein the source of said first PMOS transistor is connected to an internal standard voltage, and wherein said first PMOS transistor has the standard threshold voltage implantation but not the threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said

first test mode when said drain and said gate of said first PMOS transistor are connected to ground through a first internal standard resistance;

selecting a second PMOS transistor in said integrated circuit device in a second test mode to couple the voltage at the drain and the gate of said second PMOS transistor to said output pin of said integrated circuit device wherein said gate and said drain of said second PMOS transistor are connected together, wherein the source of said second PMOS transistor is connected to said internal standard voltage, and wherein said second PMOS transistor has both said standard threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said drain and said gate of said second PMOS transistor are connected to said ground through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

21. (Original) The method according to Claim 20 wherein said selecting of said first PMOS transistor is by a multiplex circuit and wherein said selecting of said second PMOS is by a multiplex circuit.

22. (Original) The method according to Claim 20 further comprising amplifying said voltage at said drain and said gate of said first PMOS transistor and said second PMOS transistor to thereby generate an amplified drain and gate voltage at said output pin.

23. (Original) The method according to Claim 20 wherein said first PMOS transistor and said second PMOS transistor are the same size, the same layout orientation, and in close proximity.

24. (Original) The method according to Claim 20 wherein said first internal resistance and said second internal resistance comprise the same resistance value.

REMARKS

Examiner W.D. Coleman is thanked for the thorough examination and search of the subject Patent Application.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-24 rejected under 35 U.S.C. 102(b) as being anticipated by Dasse et al (US 5,654,588) is requested based on the following remarks.

Applicant agrees that Dasse et al describes a method to manufacture and to test an integrated circuit. Further, Dasse et al appears to teach a method to fabricate identification codes for individual die on an integrated circuit wafer. In particular, in Column 8, lines 18 through 65 and Fig. 3 describe the use of identification code circuits on individual die on a wafer. Quoting from Dasse, Column 8, lines 27 through 34:

"Referring to Fig.3, integrated circuit die 27 may have an identification code circuit 67 which stores a unique identification code, and integrated circuit die 28 may have an identification code circuit 68 which stores a different

identification code. A one-to-one mapping can then be made between each Unique identification code and each available die location on the semiconductor wafer."

Further, in Column 8, lines 36 through 65, Dasse et al describes how to program the identification code either by using different masking patterns for each die (lines 41-47) or by using a programmable light source, added to the stepper apparatus, that can selectively expose photoresist without requiring different programming patterns for each die location.

Applicant, therefore, agrees with the Examiner that Dasse et al teaches a method to form identification codes on individual die. **However, the formation of identification codes is not what Applicant is claiming in the present invention as recited in Claim 1. Rather, Applicant is claiming a specific method to detect the presence (or absence) of a reticle option layer on an integrated circuit device.** In particular, Claim 1 reads:

1.(Original) A method of detecting a reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage

on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor is not parametrically affected by a reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor is parametrically affected by said reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said reticle option layer in said integrated circuit device.

Note that the claimed invention as recited in Claim 1 above teaches several key features, namely, (1) measuring currents in two MOS transistors that have been formed on a single integrated circuit device, (2) comparing these currents, and (3) making a

conclusion regarding the presence or absence of the reticle option based on this comparison.

Applicant has thoroughly studied Dasse et al, including those sections cited by the Examiner, and can find no reference to any method to read the identification code. Further, Dasse et al does not teach, suggest, or imply any testing method using two MOS transistors, measuring currents in these two MOS transistors, and then comparing these currents to obtain a conclusion regarding reticle option layers. These elements are all clearly taught in Claim 1. These elements are all clearly absent from the teachings of the cited art, Dasse et al.

It is Applicant's understanding that a finding of rejection under 102(b) against cited prior art should be made only if all of the elements of the rejected claim are taught in the cited prior art. Applicant respectfully submits that Dasse et al cannot anticipate Applicant's claimed invention as recited in Claim 1 since Claim 1 clearly contains subject matter that is not taught (anticipated) in Dasse et al. If Applicant is incorrect in this matter, it would be most helpful for the Examiner to cite actual wording from Dasse et al that demonstrates the above-described elements of the claimed invention.

In the previous Office Action of June 11, 2003, the Examiner cited Column 5, lines 65-58 and Column 6, lines 1-9, where Dasse et al makes a reference to "parametric testing". However, there is no contextual tie between the subject matter in the "parametric testing" section (col. 5, lines 65-68 and col. 6, lines 1-9) and the section (col. 8, lines 18-48) discussing ID codes. Again, Applicant quotes this section of Dasse et al (col. 5, lines 65-68 and col. 6, lines 1-9) which reads:

"There are two broad categories of electrical tests which can be performed on an integrated circuit die. The first category is functional tests. Functional tests are used to verify the logical functionality of the die independent of timing, AC characteristics, current and voltage levels, or other parametric values associated with the integrated circuit die. This test ensures that an adder adds, a multiplier multiplies, a bus using controls the bus, a memory stores bits properly, etc. The second category is parametric tests. Parametric tests are used to measure integrated circuit die characteristics over a continuous range of inputs parameters, such as voltage, current, timing, power, etc."

The first category of tests described by Dasse et al - functional, does not apply to Applicant's claimed invention because Dasse makes it clear that these tests "are used to **verify the logical functionality** of the die **independent of** timing, AC characteristics, current and voltage levels, or other **parametric values**. . ." The present invention teaches testing for a difference between parametric values and then using this difference to determine the presence/absence of a reticle option. Therefore, if anything, the functional test concept teaches against the method of Applicant's claimed invention.

The second category of tests - parametric testing - teaches measuring "integrated circuit die **characteristics** over a continuous range of inputs parameters, **such as voltage, current, timing, power,** etc." Applicant admits that such parametric testing of an IC is well-known in the art. Dasse et al is merely stating a well-known method of characterizing an IC's performance. However, Dasse does not teach or suggest in this section either the concept of, or the specific method of, performing two parametric tests to measure current on two transistors, where each transistor reacts differently to the presence of a reticle option, then comparing the test results, and then using the comparison result to determine if the reticle option was or was not used on the IC during processing. This is

the method clearly taught in Applicant's claimed invention. Again, there is no contextual tie between Dasse's reference here to parametric testing and Dasse's reference (in col. 8) to programming an ID code. Dasse simply does not tell us how to read the ID code.

Applicant, therefore, respectfully maintains that the method of determining the presence/absence of a reticle option as described in the claimed invention is not anticipated by the cited art. Applicant respectfully submits that the key features have not been demonstrated as existing in the cited art. Therefore, the cited art cannot have anticipated Applicant's claimed invention as recited in Claim 1. Applicant respectfully requests that the rejection of Claim 1 under 35 U.S.C. 102(b), as anticipated Dasse et al (US 5,654,588), be removed.

In regards to Claim 2, Claim 2 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected.

In regards to Claim 3, Claim 3 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to

reticle option layers comprising polysilicon, metal, and threshold implantation.

In regards to Claim 4, Claim 4 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to measuring two MOS transistors let alone to the size, direction, and proximity of these transistors.

In regards to Claim 5, Claim 5 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to optional reticle layers, let alone combinations of these layers.

In regards to Claim 6, Claim 6 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to optional reticle layers, let alone combinations of these layers comprising polysilicon, metal, and threshold implantation.

In regards to Claim 7, Claim 7 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to any measurement method for determining the presence or absence of the reticle, let alone a direct probing method.

In regards to Claim 8, Claim 8 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to any measurement method for determining the presence or absence of the reticle, let alone a method where the output of a packaged IC is probed.

In regards to Claim 9, Claim 9 represents a patentably distinct, further limitation on Claim 1 and should not be rejected under 35 U.S.C. 102(b) if Claim 1 is not rejected. In addition, Applicant can find no reference in Dasse et al to first and second MOS transistors used in the reticle detection method, let alone the NMOS or PMOS construction of these transistors.

In regards to Claims 10, Claim 10 recites all of the key elements recited in Claim 1 while adding additional limitations. Therefore, the above discussion with regards to the claimed invention as recited in Claim 1 also applies to the claimed invention as recited in Claim 10. Applicant respectfully requests that the rejection of Claims 10 U.S.C. 102(b), as anticipated Dasse et al (US 5,654,588), be removed for the same reasons given for Claim 1.

In regards to Claim 11, Claim 11 represents a patentably distinct, further limitation on Claim 10 and should not be rejected under 35 U.S.C. 102(b) if Claim 10 is not rejected. In addition, Applicant can find no reference in Dasse et al to measuring two MOS transistors let alone to the size, direction, and proximity of these transistors.

In regards to Claim 12, Claim 12 represents a patentably distinct, further limitation on Claim 10 and should not be rejected under 35 U.S.C. 102(b) if Claim 10 is not rejected. In addition, Applicant can find no reference in Dasse et al to any measurement method for determining the presence or absence of the reticle, let alone a direct probing method.

In regards to Claim 13, Claim 13 represents a patentably distinct, further limitation on Claim 10 and should not be rejected under 35 U.S.C. 102(b) if Claim 10 is not rejected. In addition, Applicant can find no reference in Dasse et al to any measurement method for determining the presence or absence of the reticle, let alone a method where the output of a packaged IC is probed.

In regards to Claim 14, Claim 14 represents a patentably distinct, further limitation on Claim 10 and should not be rejected under 35 U.S.C. 102(b) if Claim 10 is not rejected. In addition, Applicant can find no reference in Dasse et al to first and second MOS transistors used in the reticle detection method, let alone the NMOS or PMOS construction of these transistor.

In regards to Claims 15, Claim 15 differs from Claims 1 and 10. In Claim 15 a method is recited to indirectly measure the currents in the two MOS transistors. Here, a first internal standard resistance is connected to the drain and gate of a first NMOS transistor. A second internal standard resistance is connected to the drain and gate of a second NMOS transistor. The drain voltage of the first transistor is measured in a first test mode. The drain voltage of the second transistor is

measured in a second test mode. These voltages are compared to deduce the reticle option presence or absence. Claim 15 reads:

15. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first NMOS transistor to an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of said first NMOS transistor is connected to ground, and wherein said first NMOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when an internal test voltage is connected to said drain and said gate of said first NMOS transistor through a first internal standard resistance;

selecting a second NMOS transistor in said integrated circuit device in a second test mode to couple the voltage at the drain and the gate of said second NMOS transistor to said output pin of said integrated circuit

device wherein said gate and said drain of said second NMOS transistor are connected together, wherein the source of said NMOS transistor is connected to ground, and wherein said second NMOS transistor has both said first threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said internal test voltage is connected to said drain and said gate of said second NMOS transistor through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

As in the case of Claim 1, Applicant has thoroughly reviewed Dasse et al find the key features of the claimed invention. Applicant has not found, and the Examiner has not cited, these key features. Dasse et al does not teach using two NMOS transistors, using two internal resistors, measuring the drain voltages of the two NMOS transistors, or comparing these voltages to make a reticle conclusion. Further, the Examiner has

provided no citation from Dasse et al or rationale for this rejection. Therefore, as in Claims 1 and 10, Applicant respectfully requests that the rejection of Claims 15 U.S.C. 102(b), as anticipated Dasse et al (US 5,654,588) be removed.

In regards to Claim 16, Claim 16 represents a patentably distinct, further limitation on Claim 15 and should not be rejected under 35 U.S.C. 102(b) if Claim 15 is not rejected. In addition, Applicant can find no reference in Dasse et al to a multiplex circuit and, more particularly, a multiplex circuit used in conjunction with a method to determine reticle option presence.

In regards to Claim 17, Claim 17 represents a patentably distinct, further limitation on Claim 15 and should not be rejected under 35 U.S.C. 102(b) if Claim 15 is not rejected. In addition, Applicant can find no reference in Dasse et al to amplifying the first and second NMOS drain voltages.

In regards to Claim 18, Claim 18 represents a patentably distinct, further limitation on Claim 15 and should not be rejected under 35 U.S.C. 102(b) if Claim 15 is not rejected. In addition, Applicant can find no reference in Dasse et al to

measuring two MOS transistors let alone to the size, direction, and proximity of these transistors.

In regards to Claim 19, Claim 19 represents a patentably distinct, further limitation on Claim 15 and should not be rejected under 35 U.S.C. 102(b) if Claim 15 is not rejected. In addition, Applicant can find no reference in Dasse et al to using first and second internal resistors.

In regards to Claims 20, Claim 20 is substantially similar to Claim 15 with additional limitations. Therefore, Applicant's observations regarding Claim 15 apply also to Claim 20. Applicant has thoroughly reviewed Dasse et al find the key features of the claimed invention as described in Claim 20. Applicant has not found, and the Examiner has not cited, these key features. Dasse et al does not teach using two NMOS transistors, using two internal resistors, measuring the drain voltages of the two NMOS transistors, or comparing these voltages to make a reticle conclusion. Further, the Examiner has provided no citation from Dasse et al or rationale for this rejection. Therefore, as in Claims 1 and 10, Applicant respectfully requests that the rejection of Claims 20 U.S.C. 102(b), as anticipated Dasse et al (US 5,654,588) be removed.

In regards to Claim 21, Claim 21 represents a patentably distinct, further limitation on Claim 20 and should not be rejected under 35 U.S.C. 102(b) if Claim 20 is not rejected. In addition, Applicant can find no reference in Dasse et al to a multiplex circuit and, more particularly, a multiplex circuit used in conjunction with a method to determine reticle option presence.

In regards to Claim 22, Claim 22 represents a patentably distinct, further limitation on Claim 20 and should not be rejected under 35 U.S.C. 102(b) if Claim 20 is not rejected. In addition, Applicant can find no reference in Dasse et al to amplifying the first and second NMOS drain voltages.

In regards to Claim 23, Claim 23 represents a patentably distinct, further limitation on Claim 20 and should not be rejected under 35 U.S.C. 102(b) if Claim 20 is not rejected. In addition, Applicant can find no reference in Dasse et al to measuring two MOS transistors let alone to the size, direction, and proximity of these transistors.

In regards to Claim 24, Claim 24 represents a patentably distinct, further limitation on Claim 20 and should not be rejected under 35 U.S.C. 102(b) if Claim 20 is not rejected. In

addition, Applicant can find no reference in Dasse et al to using first and second internal resistors.

Finally, Applicant has carefully reviewed the citations of Dasse et al that have been provided by the Examiner. Applicant respectfully notes that these citations do not appear to contain the specific features of Applicant's claimed invention that the Examiner is rejecting. Further, Applicant has carefully reviewed all of Dasse et al yet has been unable to find these features anywhere in it's specification and/or drawings. Therefore, Applicant respectfully requests that the Examiner provide more specific citations from Dasse et al that show these features as an aid to understanding the rationale of these rejections and/or to provide a basis for amending the claims to remove these rejections.

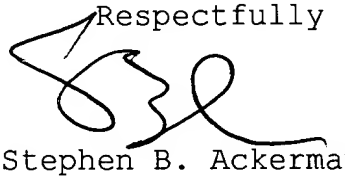
Reconsideration of Claims 1-24 rejected under 35 U.S.C. 102(b) as being anticipated by Dasse et al (US 5,654,588) is requested based on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,



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